AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

1. (Currently Amended) A microprocessor built on a semiconductor chip comprising:

a central processing unit for executing instructions; [[and]]

an external bus interface control circuit, coupled to said central processing unit, which controls an external bus ~~on the basis of~~ based on execution of instructions by said central processing unit, ~~wherein said external bus interface control circuit~~ said external bus interface control circuit being ~~is~~ capable of selecting one of a plurality of external device select signals corresponding to an external access address and activating said selected external device select signal; [[, and]]

~~wherein said microprocessor further comprises~~ a clock generating circuit, coupled to said central processing unit and said external bus interface control circuit, to generate a plurality of clock signals;

a clock switching control circuit for controlling an operation to switch a synchronous clock signal [[of]] provided to said external bus interface control circuit in accordance with said external device select signal activated by said external bus interface control circuit;

a first clock terminal, coupled to said clock generating circuit, to supply a first clock signal to a first external device; and

a second clock terminal, coupled to said clock generating circuit, to supply a second clock signal to a second external device, in parallel with said first clock signal, said second clock signal having a different frequency from said first clock signal.

2. (Currently Amended) A microprocessor comprising:

a central processing unit for executing instructions; and

an external bus interface control circuit which controls an external bus ~~on the basis of~~ based on execution of instructions by said central processing unit,

wherein said external bus interface control circuit is capable of activating either a first external device select signal or a second external device select signal corresponding to an external access address, [[and]]

wherein said microprocessor ~~comprises~~ includes a clock switching control circuit and a clock pulse generator,

wherein said clock switching control circuit controls ~~for controlling~~ an operation to switch a synchronous clock signal of said external bus interface control circuit to a first clock signal in accordance with activation of said first external device select signal or to a second clock signal in accordance with activation of said second external device select signal, and

wherein said clock pulse generator generates said first clock signal and said second clock signal, and said first clock signal is a predetermined frequency different from that of second clock signal.

3. (Currently Amended) [[A]] The microprocessor according to claim 2,

wherein said microprocessor further comprises ~~a clock pulse generator and~~ clock output pins, and

~~wherein said clock pulse generator generates said first clock signal and said second clock signal with a period equal to a predetermined multiple of the period of said first clock signal where said predetermined multiple~~

~~is defined as a quantity equal to a frequency-division ratio, and~~

wherein said clock output pins supply respectively said first and second clock signals generated by said clock pulse generator in parallel ~~to respectively outside~~.

4. (Currently Amended) A microprocessor comprising:

a central processing unit for executing instructions; [[and]]

an external bus interface control circuit controlling an external bus ~~on the basis of~~ based on execution of instructions by said central processing unit, wherein said external bus interface control circuit is capable of activating either a first external device select signal or a second external device select signal corresponding to an external access address~~,~~; and

~~wherein said microprocessor further comprises~~ a clock switching control circuit, ~~wherein said clock switching control circuit is~~ capable of:

~~controlling to~~ switching [[said]] a synchronous clock signal of said external bus interface control circuit to [[said]] a first clock signal ~~as well as switch~~ and a synchronous clock signal of said central processing unit to a third clock signal in response

to activation of said first external device select signal, and

~~is capable of controlling to~~ switching said synchronous clock signal of said external bus interface control circuit to [[said]] a second clock signal ~~as well as switch~~ and said synchronous clock signal of said central processing unit to a fourth clock signal in response to activation of said second external device select signal,

wherein a frequency of said first clock signal is different from a frequency of said third clock signal, a frequency of said second clock signal is different from a frequency of said fourth clock signal and said first clock signal and said second clock signal are provided in parallel and external to the microprocessor.

5. (Currently Amended) [[A]] The microprocessor according to claim 4,

wherein said microprocessor further comprises a clock pulse generator and clock output pins,

wherein said clock pulse generator generates said first clock signal, said second clock signal, said third clock signal and said fourth clock signal, ~~with a period equal to a predetermined multiple of the period of said~~

~~first clock signal where said predetermined multiple is defined as a quantity equal to a frequency-division ratio, said third clock signal and said fourth clock signal with a period equal to another predetermined multiple of the period of said third clock signal where said other predetermined multiple is defined as a quantity equal to another frequency-division ratio,~~

wherein said clock output pins output respectively said first and second clock signals generated by said clock pulse generator ~~to respectively outside [[said]]~~ a ~~semiconductor chip~~, and

wherein [[said]] each of ~~frequencies of~~ said third and fourth clock signal frequencies is that of said first clock signal.

6. (Currently Amended) [[A]] The microprocessor according to claim 2,

wherein said clock switching control circuit requests said central processing unit to suspend execution of instructions in response to activation of a selected external device select signal, and

wherein said clock switching control circuit is further capable of ~~controlling to~~ switching said clock signal which is provided to said external bus interface

control circuit, after an acknowledgment of ~~a~~ the request ~~for~~ to suspend[[ing]] ~~of said~~ instruction execution.

7. (Currently Amended) [[A]] The microprocessor according to claim 6, wherein said clock switching control circuit is capable of ~~controlling to~~ switching said clock signal ~~at a timing synchronized with periods of said second clock signal~~ of said central processing unit in accordance with switching said clock signal of said external bus interface control circuit.

8. (Currently Amended) A semiconductor module on a module substrate including a plurality of external connection electrodes and a plurality of wiring layers, the semiconductor module comprising:

a microprocessor chip including a clock pulse generator for generating a first clock signal, a second clock signal and a third clock signal; and

a memory chip operating synchronously with ~~a~~ the first clock signal,

wherein ~~said microprocessor chip includes a clock pulse generator for generating said first clock signal and~~ ~~a~~ said second clock signal ~~with~~ has a frequency lower than ~~that of~~ said first clock signal,

wherein said third clock signal has a frequency different from said first clock signal and different from said second clock signal, [[and]] ~~for~~

wherein said clock pulse generator supplies, ~~supplying~~ in parallel, said first and second clock signals ~~to outside~~external to said microprocessor chip,

wherein said microprocessor chip is capable of ~~making an access~~ accessing ~~to~~ said memory chip synchronously with said first clock signal, and

wherein said microprocessor chip is capable of ~~making an external access to outside of said microprocessor chip through one of external connection electrodes~~ accessing an external device synchronously with said second clock signal.

9. (Currently Amended) [[A]] The semiconductor module according to claim 8,

wherein said microprocessor chip comprises:

a central processing unit for executing instructions and for operating based on said third clock signal; and

an external bus interface control circuit for controlling an external bus ~~on the basis of~~ based on execution of an instruction by said central processing unit,

wherein said central processing unit and said external bus interface control circuit are built in a single chip,

wherein said external bus interface control circuit is capable of activating a memory chip select signal for selecting said memory chip in response to an external access address and an external device select signal for selecting an external device connected to said microprocessor chip through one of said external connection electrodes,

wherein said microprocessor chip ~~comprises~~ includes a clock switching control circuit~~, wherein said clock switching control circuit is~~ capable of:

~~controlling to~~ switching a synchronous clock signal of said external bus interface control circuit to a first clock signal in response to activation of said memory chip select signal, ~~or is capable of controlling to~~ and

switching said synchronous clock signal of said external bus interface control circuit to a second clock signal in response to activation of said device select signal.

10. (Currently Amended) A data-processing system comprising:

a first ~~clock~~ signal wire for transferring a first ~~clock~~ pulse signal;

a second ~~clock~~ signal wire for transferring a second ~~clock~~ pulse signal with a frequency lower than said first ~~clock~~ pulse signal;

a first device operating ~~synchronously~~ in accordance with said first ~~clock~~ pulse signal applying through said first ~~clock~~ signal wire;

a second device operating ~~synchronously~~ in accordance with said second ~~clock~~ pulse signal; and

a third device capable of controlling accesses to said first device ~~synchronously~~ in accordance with said first ~~clock~~ pulse signal and capable of controlling accesses to said second device ~~synchronously~~ in accordance with said second ~~clock~~ pulse signal,

wherein said third device generates said first pulse signal, said second pulse signal and a third pulse signal, and

wherein said first ~~clock~~ signal wire, said second ~~clock~~ signal wire, said first device, said second device and said third device are provided on a mounting board.

11. (Currently Amended) [[A]] The data-processing system according to claim 10, wherein said mounting board comprises:

a first circuit board including a first board wire ~~connected~~ coupled to said second device; and

a second circuit board including a second board wire ~~connected~~ coupled to said first board wire, ~~and said second board wire is connected to~~ said first device and a third device.

12. (Currently Amended) [[A]] The data-processing system according to claim 10,

wherein said third device is a microprocessor on a single semiconductor chip comprising a central processing unit for executing instructions, an external bus interface control circuit for controlling an external bus ~~on the basis of~~ based on execution of instructions by said central processing unit,

wherein said external bus interface control circuit is capable of activating a first external device select signal for selecting said first device or a second external device select signal for selecting said second device in accordance with an external access address,

wherein said third device further includes a ~~clock~~ switching control circuit, and

wherein said ~~clock~~ switching control circuit is capable of ~~controlling to~~ switching a pulse ~~a synchronous clock~~ signal of said external bus interface control circuit to:

[[a]] said first ~~clock~~ pulse signal in response to activation of said first external device select signal, and

to ~~or is capable of controlling to switch said synchronous clock signal of said external bus interface control circuit to a~~ said second ~~clock~~ pulse signal in response to activation of said second external device select signal.

13. (Currently Amended) [[A]] The data-processing system according to claim 12,

wherein said third device further comprises a pulse signal control circuit ~~clock pulse generator~~ and ~~clock~~ pulse signal output pins,

wherein said pulse signal control circuit ~~clock pulse generator applies~~ generates said first ~~clock~~ pulse signal and said second ~~clock~~ pulse signal, said first and second pulse signals being different from said third pulse signal

~~with a period equal to a predetermined multiple of the period of said first clock signal where said predetermined multiple is defined as a quantity equal to a frequency-division ratio~~, and

wherein said ~~clock~~ pulse signal output pins apply ~~applies respectively~~ said first and second ~~clock~~ pulse signals ~~generated by said clock pulse generator~~ in parallel ~~to outside said semiconductor chip~~to said first device and second devices, respectively.

14. (Currently Amended) A microprocessor according to claim 4,

wherein said clock switching control circuit requests said central processing unit to suspend execution of instructions in response to activation of a selected external device select signal, and

wherein said clock switching control circuit is further capable of ~~controlling to~~ switching ~~said clock signal~~ said first clock signal and said second clock signal to said external bus interface control circuit after an acknowledgment of the request for suspending of said instruction execution.